We claim:

1. A method of fabricating a reconfigurable processor for running moderately complex programming applications comprising:

(a) providing source code for a programming application,

(b) entering the source code in a control flow graph generating compiler to produce a control data flow graph of data flow control flow and branch points,

(c) extracting form the control flow graph basic blocks of code lying between branch points,

(d) from the code lying between the branch points generating intermediate data flow graphs,

(e) identifying clusters shared among dfgs at the highest level of granularity,

(f) from the identified clusters determine the largest common subgraph shared among the dfgs,

(g) scheduling the largest common subgraph for fast accomplishment of operations in the lcsg,

(h) apply the scheduled lcsg to the intermediate flow graphs replacing the unscheduled lcsg therein,

(i) scheduling the intermediate flow graphs containing the lcsg's for fast accomplishment of operations in the intermediate flow graphs to derive data patches having operations and timings of each intermediate flow graph,

(j) combining the data patches to include operations and timing of the lcsg with operations and timings of each intermediate subgraph that are outside the lcsg,

(k) from the combined data patches scheduling for process time reduction multiple uses of the lcsg operations and timings necessary to accomplish operations and timings of all intermediate subgraph employing the lcsg , and

(l) implementing in hardware having mixed granularities the operations and timing of the lcsg including:

(i) partitioning,

(ii) placing, and

(iii) interconnection routing.

2. In a method of making an integrated circuit for use as a hardware implemented part of a programmed operation implemented in software and hardware; the improvement comprising identifying hardware circuit elements for execution of a largest common subgraph common among a set of flow graphs representing the programmed operation; partitioning into blocks the circuit elements; arranging the blocks on an area representative of an available area of a surface of a substrate on which the circuit elements are to be formed; routing interconnections among the blocks; partitioning into sub-blocks the circuit elements of each block; arranging each sub-block on an area representative of the block form which it has been partitioned routing interconnections among the sub-blocks and iteratively partitioning and routing among lesser sub-blocks until the individual circuit elements have been placed and routed.

3. The method according to claim 2, wherein the steps of routing comprise locating conductors and switches for interconnections among blocks, sub-blocks and circuit elements.

4. The method according to claim 3, wherein locating conductors and switches further comprises locating variable switches to effect variable conductive paths among the blocks, sub-blocks and circuit elements.

5. A method of scheduling process elements of hardware implementing a software application, comprising:

(a) developing a control data flow graph from the software;

(b) using a first, non-exhaustive scheduling algorithm to relatively quickly arrive at a first scheduling of the process elements;

(c) using a second more exhaustive scheduling algorithm for at least one and less than all selected paths of the control data flow graph to reduce the time of execution thereof; and

(d) once all paths of the control data flow graph have been scheduled, including all of the second more exhaustive scheduling, merge all of schedules, respecting data and resource dependencies.

6. The method of scheduling according to claim 5, wherein step (a) comprises PCP scheduling.

7. The method of scheduling according to either claim 5 or 6, wherein step (b) comprises branch and bound based scheduling.

8. A dedicated integrated circuit for performing the software operation having processing elements scheduled according to claim 5.

9. A dedicated integrated circuit for performing the software operation having processing elements scheduled according to claim 6.

10. A dedicated integrated circuit for performing the software operation having processing elements scheduled according to claim 7.

1. The method of forming an application specific reconfigurable circuit, comprising:

(a) providing source code for an application to be run b the circuit,

(b) deriving flow graphs representing separate portions of the application,

(c) identifying at least one largest common flow graph from at least two of the separate portions of the application; and

(d) configuring in hardware circuitry to be shared by the separate portions of the application.